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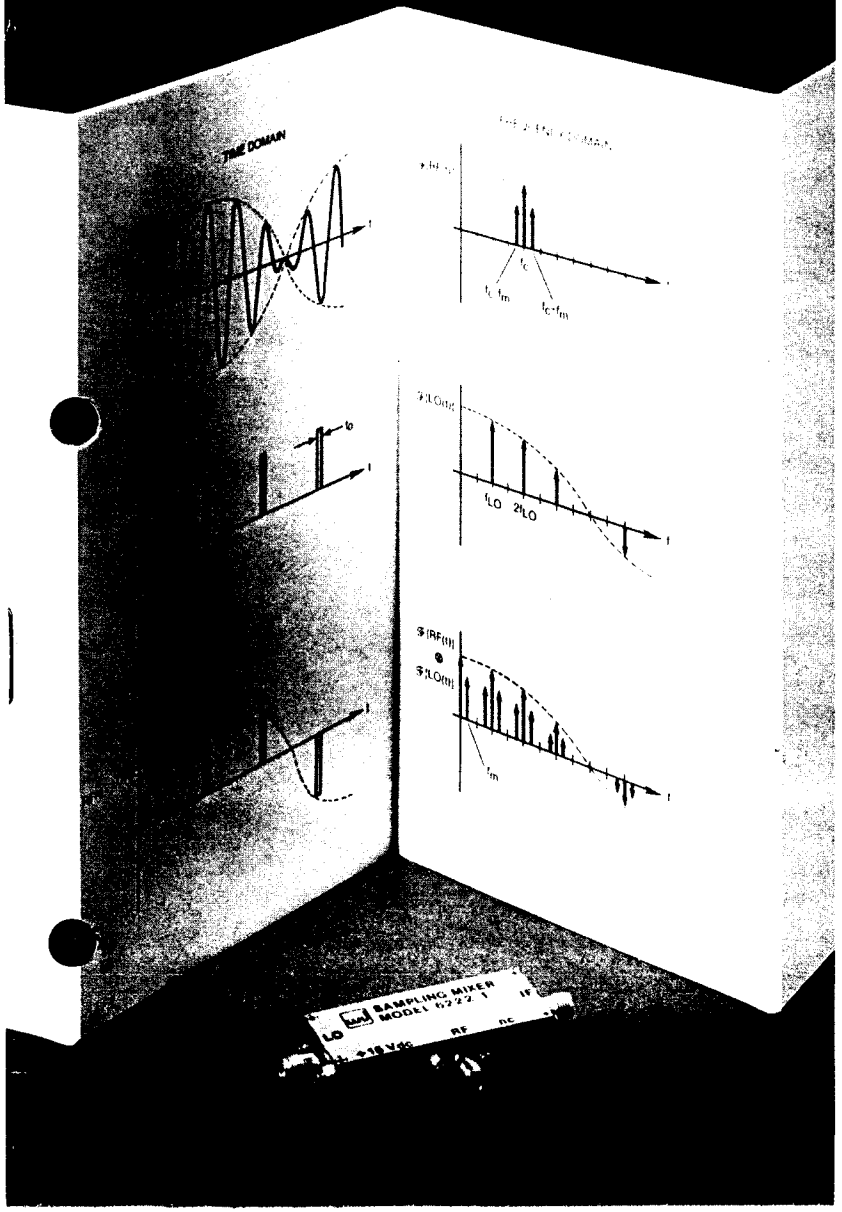
Microwave Sampling for Ultra-Broadband Frequency Conversion



Tech-notes

In many microwave phase-locking systems there exists a need for an ultra-broadband frequency converter. Broadband downconversion has typically been implemented using YIG multipliers or harmonic generators, both of which rely on generating harmonics of a synthesized UHF signal to be used as the local oscillator (LO) for a standard wideband mixer.

A microwave sampler, relying on time-domain sample-and-hold techniques, eliminates the additional circuitry associated with harmonic generation and, therefore, simplifies system design. It is capable of downconverting any RF signal up to and beyond 18 GHz to a low-frequency IF (typically less than 500 MHz), while only requiring sampling rates in the 50 to 2000 MHz frequency range, where highly stable sources are available.

For many years, samplers have been used almost exclusively in instrumentation applications, such as microwave frequency counters, broadband voltmeters, network analyzers, oscilloscopes, etc.[1] Recently, their usage in military systems, such as found in phase-locking synthesizers, has become a reality. The WJ SN-701 Synchronizer (see Figure 1) is one example of a military system that uses sampling techniques for downconverting signals of up to 20 GHz.

The following will provide the system designer with a general introduction to the use of sampling techniques. A typical application and sampler benefits, as well as general sampling theory will be presented along with a description of the hardware involved and the results obtained.

Downconverter Applications

In many downconverting systems, such as found in phase-locked synthesizers or receivers, there is a need for a small, efficient and wideband downconverter. A typical systems application might be the synthesizer whose block diagram is shown in Figure 2. A portion of the microwave output is downconverted and divided to enable

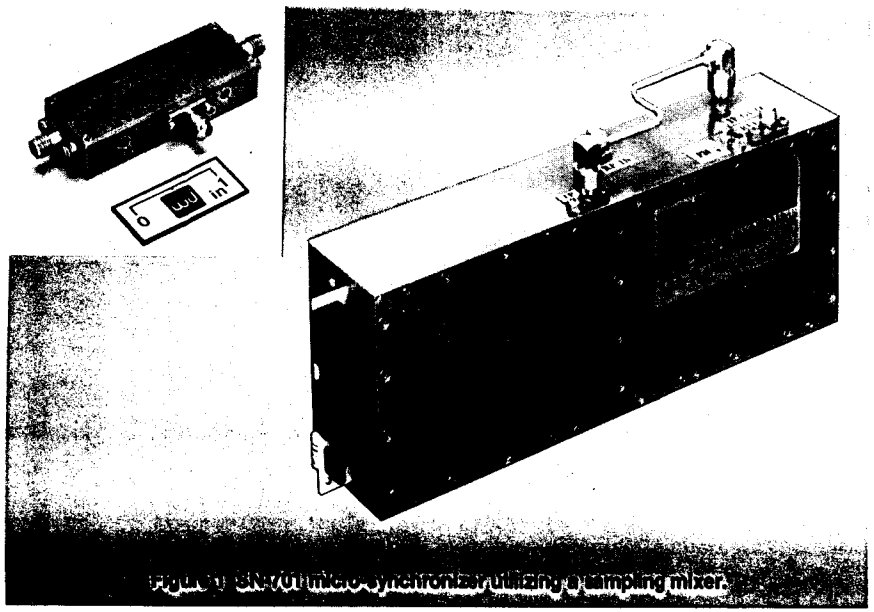


Figure 1. SN-701 micro-synchronizer utilizing a sampling mixer.

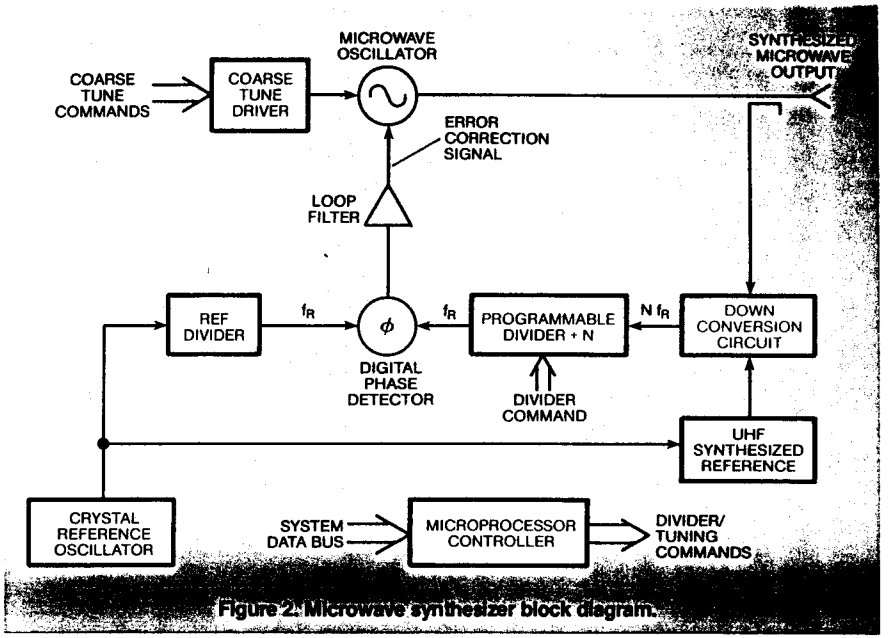


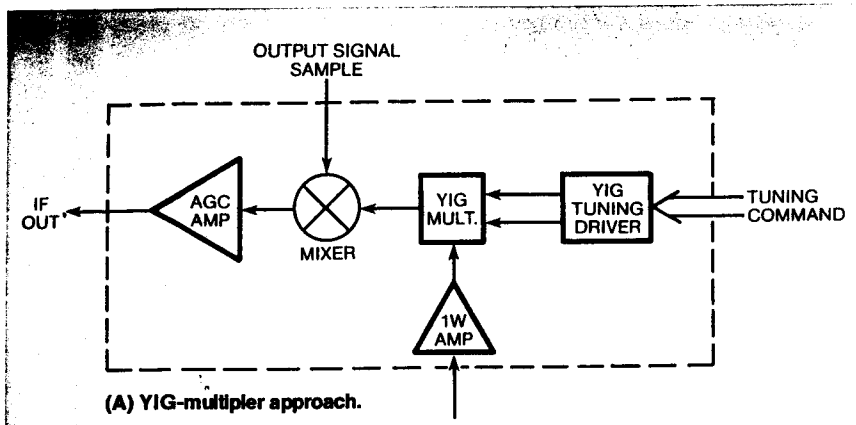
Figure 2. Microwave synthesizer block diagram.

comparison with a crystal reference so that a frequency-correcting error signal can be generated. The UHF synthesizer that drives the downconverter must be extremely stable if the error signal in the feedback loop is to be due to frequency variations in the microwave output only, and not to frequency variations of the local oscillator. Both the YIG multiplier and the harmonic mixer rely on harmonics of the narrowband UHF synthesizer to function as the local oscillator for a standard wideband mixer.

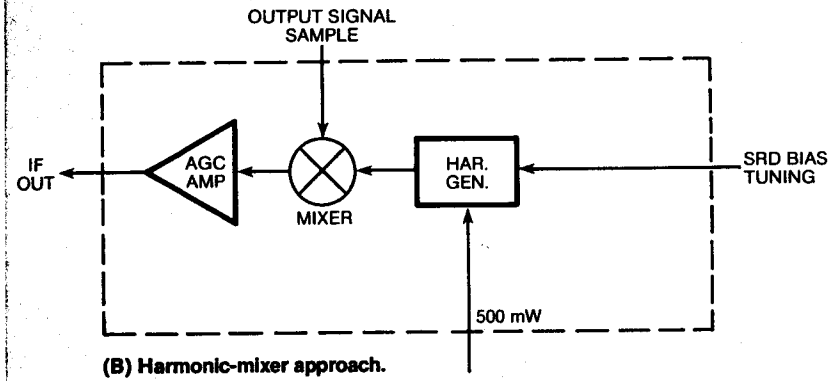
Some of the disadvantages of the YIG-multiplier approach (see Figure 3A) are that it typically requires a 1-watt reference signal, must be tuned to the desired RF frequency, and dissipates large amounts of heat. The YIG multiplier's size and weight also limit its usefulness in miniature applications. The harmonic mixer (see Figure 3B) *does* reduce size and power requirements, as well as improve reliability, but requires SRD (step recovery diode) bias adjustments to maintain frequency lock over broad bandwidths, thus slowing operation. Both approaches exhibit a wide range of conversion losses versus RF frequency, which necessitates some kind of AGC (automatic gain control) amplification.

The sampler approach (see Figure 3C), by utilizing time-domain properties as its fundamental design approach, has been shown capable of overcoming all of the aforementioned operational problems, while also requiring less hardware, which lowers system cost. It consumes less volume, less power, requires no bias tuning or AGC amplification, and requires no microprocessor interaction to optimize conversion loss. It is much less dependent on frequency-domain effects, and has been shown to operate across the entire 2 to 18 GHz band, and even up to 40 GHz.[2]

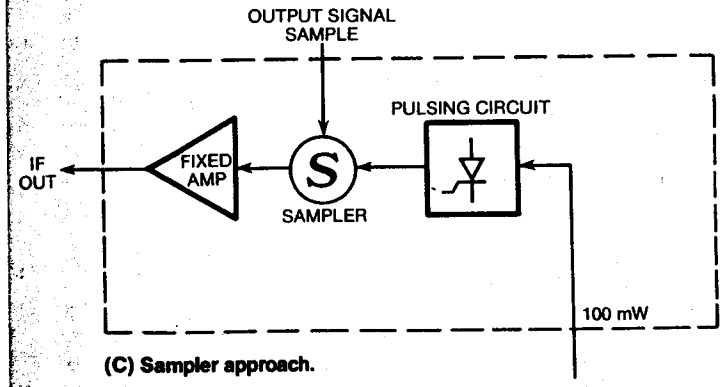
When using the harmonic-generating method of downconversion, or using sample-and-hold techniques as



(A) YIG-multiplier approach.



(B) Harmonic-mixer approach.



(C) Sampler approach.

Figure 3. Down-conversion block diagram.

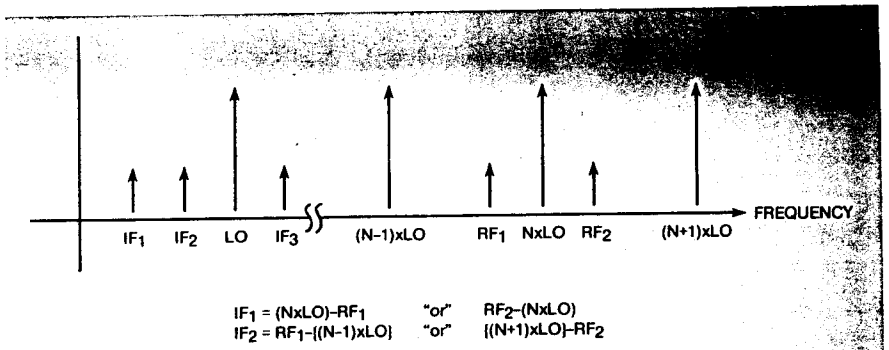


Figure 4. Down-conversion products.

described in a later section, any and all signals present within the RF operational bandwidth will be mixed to an IF baseband. Since the IF frequency is determined by,

$$IF = RF \pm (NxLO)$$

(see Figure 4), it is possible that two different RF signals may be down-converted to the same IF frequency if they are equally spaced from an LO harmonic. The problem of determining with which harmonic the RF signal has mixed is solved in instrumentation applications by slightly modifying the LO frequency. By taking two IF frequency measurements and noting in which direction the IF moved (i.e., up or down in frequency when the LO is increased), the harmonic number and RF frequency can be calculated. For general downconverting systems, then, it becomes necessary to have a well-defined or restricted signal. These are the types of signals typically found in microwave instrumentation, phase-locked synthesizers, and other similar systems.

Sampling Theory

In digital signal-processing schemes, an analog input signal is generally digitized or pulse-amplitude modulated (PAM) using a sample-and-hold circuit before being processed. The basis for this type of modulation is that if the sampling rate is chosen according to the Nyquist criterion, then the original analog signal may be reconstructed using an ideal low-pass filter. Sampling theory can be extended to bandpass signals greater than the sampling frequency,[4] with the result being a periodic translation of the input spectrum starting at dc.

Consider a bandpass signal consisting of any RF frequency from 2 to 18 GHz with a bandwidth, $2f_m$. The RF signal will be sampled at the LO frequency.* Figure 5 shows the time and frequency domain representation of a simple exemplary signal. The most important parameter is the sampling pulse width, t_o. Ideally, t_o would go to zero, making the sampling pulse singular, and the output would contain repeated replicas of the RF input up to infinite frequency. Because t_o is finite, the output spectra is of the form, (sin f)/f; obtained from the convolution of $\mathcal{F}\{LO(t)\}$ and $\mathcal{F}\{RF(t)\}$. The crossover point where, $\mathcal{F}\{LO(t)\} = 0$, must be greater than the highest RF frequency. For 18-GHz operation, this constrains t_o to be less than approximately 40 ps. The other parameter of interest is the sampling repetition rate or, equivalently, the local oscillator frequency. It must be high enough to

*The familiar mixer term, LO, is used to represent the sample signal, even though the "LO" in a sampler serves a fundamentally different purpose than it does in a mixer.

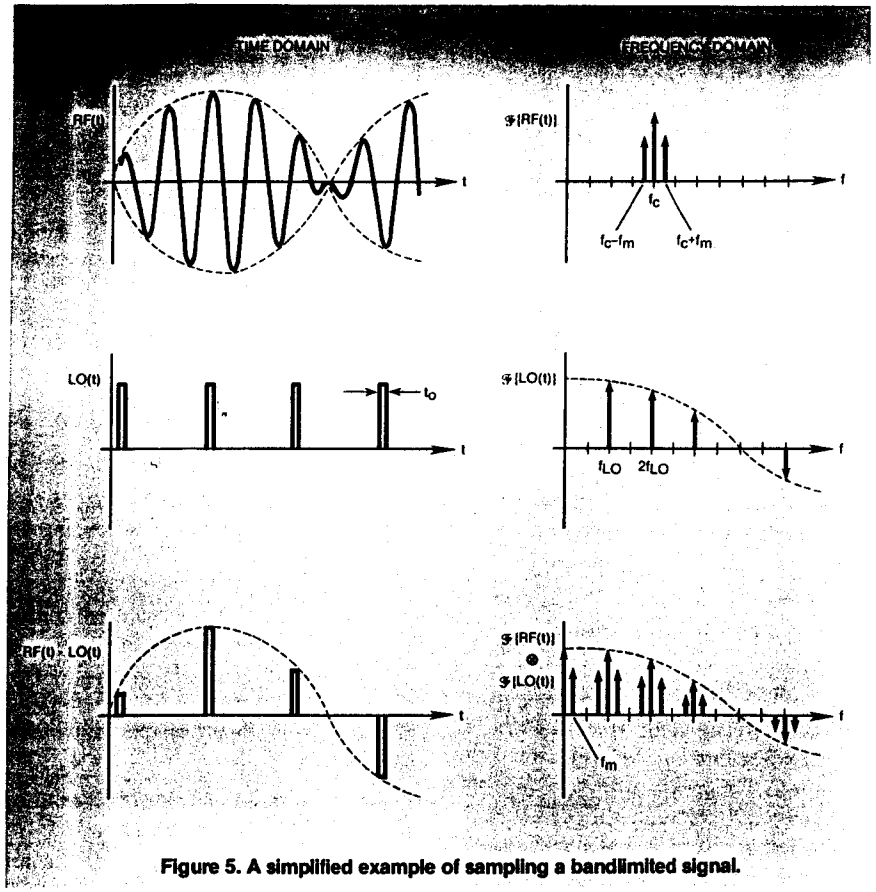


Figure 5. A simplified example of sampling a bandlimited signal.

avoid aliasing (i.e., the overlap of any converted RF sidebands); yet, for practical reasons, would preferably be as low as possible. A typical sampling rate might be in the 100 to 1000 MHz range, generally chosen as an integral fraction of the RF carrier frequency so that the modulation sidebands are downconverted to an IF baseband centered at dc.

In summary, an LO signal can be used to generate sampling pulses (utilizing a SRD pulsing circuit described later in this paper) of the appropriate pulsewidth and frequency which, when used to sample an RF signal, will generate replicas of the RF signal starting at dc.

A simplified model of the sampling circuit is shown in Figure 6. The high-level LO signal closes the switch for t_o ps, at which time the sampling capacitor, Cs, charges up to the value of the RF signal. After the switch opens, the capacitor discharges and the process repeats itself.

Pulsing Circuit

The approach taken to generate the very narrow sampling pulse is to utilize the step recovery diode (SRD). An SRD is a PIN diode that is capable of switching from its conducting state to nonconduction in an extremely short amount of time. The diode intrinsic layer causes

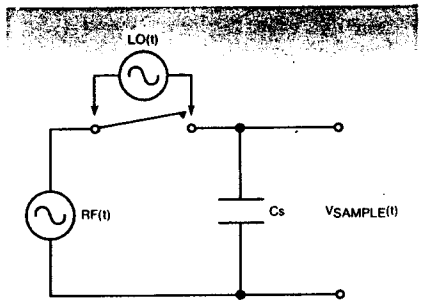


Figure 6. Sampler model.

the diode capacitance to assume one of two states. When the diode is "on" it is modeled as a large capacitance (i.e., approximately a short circuit), and when it is "off," it is modeled as a very small capacitance (approximately an open circuit). In most cases, the capacitance can be assumed to be independent of voltage. The two well-defined states permit a double-linear analysis of the SRD pulsing circuit shown in Figure 7.

When the input voltage goes positive, the SRD turns on (see Figure 7B), generating one diode junction voltage drop at the output. While the diode is on, it stores charge in its intrinsic region. When the applied voltage starts to go negative, it takes a finite amount of time for this charge to decrease, at which time the diode will turn off. Before the diode turns off though, it will continue conducting current as if it were a short. This means that for a short time there will be reverse current through the diode when V_{lo} (t) goes negative. This reverse current causes the stored charge to gradually decrease. Once the charge has been removed, the diode quickly changes to its high-impedance state (see Figure 7C). The dc bias voltage is used to cause the current to be at its maximum negative value when the diode turns off. When the diode goes off, current, which cannot change instantaneously, is still flowing through the inductor. As a result, a current surge flows through the load. If

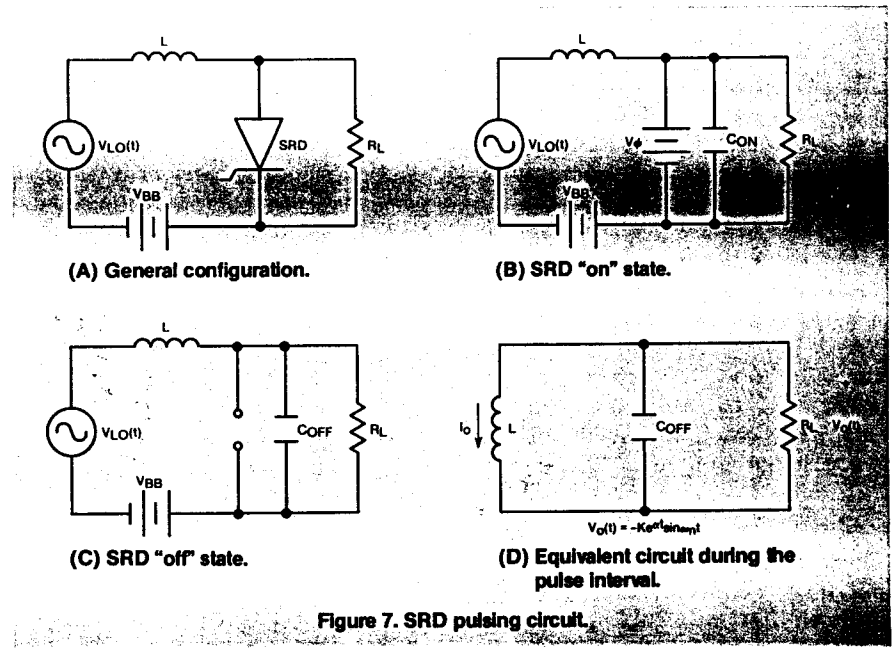


Figure 7. SRD pulsing circuit.

the bias voltage is chosen correctly, then the current and, therefore, the pulse amplitude, will be at a maximum. The circuit can then be analyzed as a parallel RLC circuit driven with an initial inductor current, I_o (see Figure 7D). From linear circuit theory, the natural frequency (w_n) can be found for this damped waveform.

The SRD is still physically connected, so as soon as the output tries to go positive, it will turn on again, shorting the output. The final result is a single negative-going pulse, its width being determined by the proper choice of L, R and C_{off}.

$$w_n = \frac{2\pi}{Tn} = \frac{2\pi}{2t_p} = \frac{\pi}{t_p}$$

where: w_n = RLC natural frequency
t_p = pulsewidth

Two parameters constrain the choice of SRD to be used. The SRD transition time (t_t) is the time the diode takes to turn off after all of its charge has been removed. Its value must be less than the period of the highest RF frequency to be encountered. The other parameter is minority-carrier lifetime (τ), which is a measure of how long a mobile carrier will last in the SRD bulk before recombination takes place. To ensure that the carriers are affected by the changing LO potential across the SRD and not by carriers recombining, τ should be much greater than the period of the LO signal. For operation to 18 GHz, the transition time, t_t, is typically on the order of 50 ps, while the minority-carrier lifetime, τ, is about 20 ns for a 100-MHz sampling rate.

Sample-and-Hold Circuit

The pulse generated by the SRD pulsing circuit is used to turn on a Schottky diode so that the sampling capacitor (Cs) can charge up to the value of the RF signal. The technology used for thin-film mixers can be utilized for the sampler circuitry and has several advantages. Mixers are typically designed using a specific combination of microstrip and coplanar waveguide transmission lines to feed the RF and LO to the mixer diodes. The sampler utilizes a similar structure, but relies on an effective short circuit at the microstrip-to-CPW transition. The shorted transmission line will reflect the incident pulse, with the reflected pulse being 180° out of phase. This opposite polarity pulse can be used to turn the sampler diodes "off." The effective sampling pulsewidth will then be even shorter in duration than the pulse generated by the SRD. The important parameter of the pulsing circuit then becomes the negative-going edge of the SRD-generated pulse.

The sampler circuit is shown in Figure 8. The SRD pulse is applied to a 50-ohm microstrip line which is terminated at its end. On the back side of the substrate is a coplanar waveguide (CPW) line which will propagate the RF. The RF microstrip-to-CPW transition will only launch the odd mode of propagation in the CPW. The sampling operation is performed by turning on the two Schottky diodes with the SRD pulse and letting the sampling capacitors charge up to the RF signal level present on the CPW line. Figure 8A shows the basic microstrip-to-CPW transition. The sampling diodes and capacitors are mounted on the backside across each gap in the CPW line. The RF on the CPW is terminated at its end also.

The sampling capacitors will charge up to some value determined by the level of the SRD pulse, and then the RF will increase the charge on Cs2, but decrease the charge on Csl (when the RF is positive). This balanced approach helps to keep the LO from coupling through

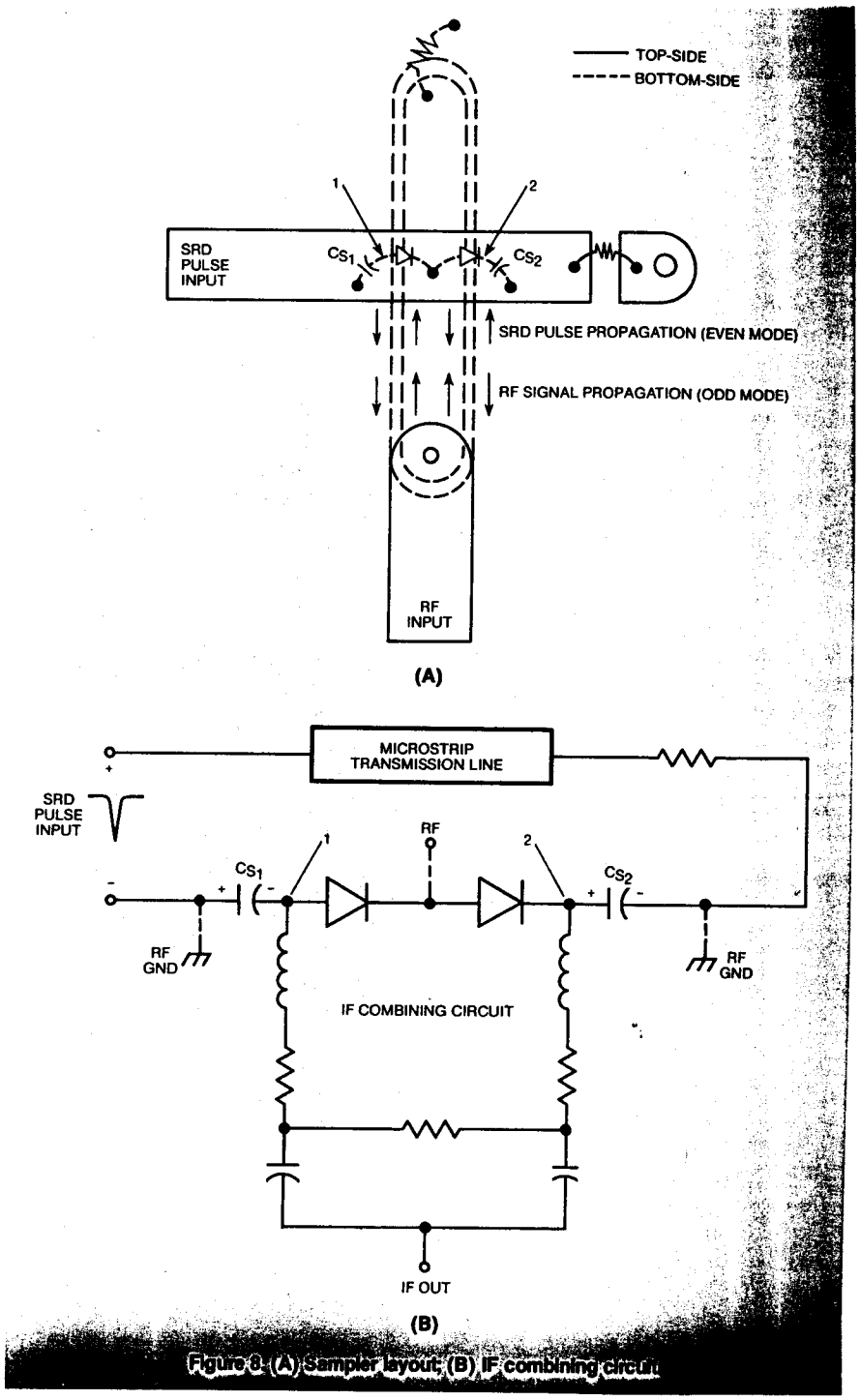


Figure 8. (A) Sampler layout; (B) IF combining circuit.

to the RF input line. The differential voltage between these two points is then converted to a single-ended IF signal using an IF combining circuit (see Figure 8B). The IF output is then a low-frequency replica (usually at VHF) of the RF signal.

The time the sampler diodes are "on" can be seen by examining Figure 8A. The RF microstrip-to-CPW transition will launch an odd-mode signal only. The SRD pulse will couple to the CPW line in an even mode of propagation. This even-mode signal sees a short at the RF microstrip-to-CPW transition, and reflects back an opposite polarity signal. The diodes will be turned "off" after the time it takes to propagate up to and back from this transition. This length was designed for a round-trip propagation time of approximately 30 ps.

Integrated Sampler

A block diagram of a complete sampler is shown in Figure 9. Two versions will be described. The WJ-6221-2 operates with an LO of 1200 to 1500 MHz, at +10 dBm, while the WJ-6222-1 operates with an LO input of 60 to 70 MHz, at -3 dBm.

The major design difference between the two units is in the pulsing circuit.[5] The higher frequency pulsing circuit requires a matching circuit at its input because of the extremely low equivalent impedance of the SRD when driven at L-band frequencies. The lower frequency pulsing circuit has an equivalent impedance close to 50 ohms, and is operable without any matching circuitry. The SRD-generated pulse is shown in Figure 10 for the two LO-frequency designs. The trailing edge of the low-frequency design was found to be caused by the short minority-carrier lifetime of the SRD, compared to the period of the LO. Since only the leading edge of the pulse is of concern, as discussed previously, it poses no problem when operated in the complete circuit of Figure 9. The SRD is also the temperature-sensitive element of the sampling mixer. The temperature-compensation circuitry compensates for the changing minority-carrier lifetime over temperature by altering the dc bias voltage as necessary. The circuit

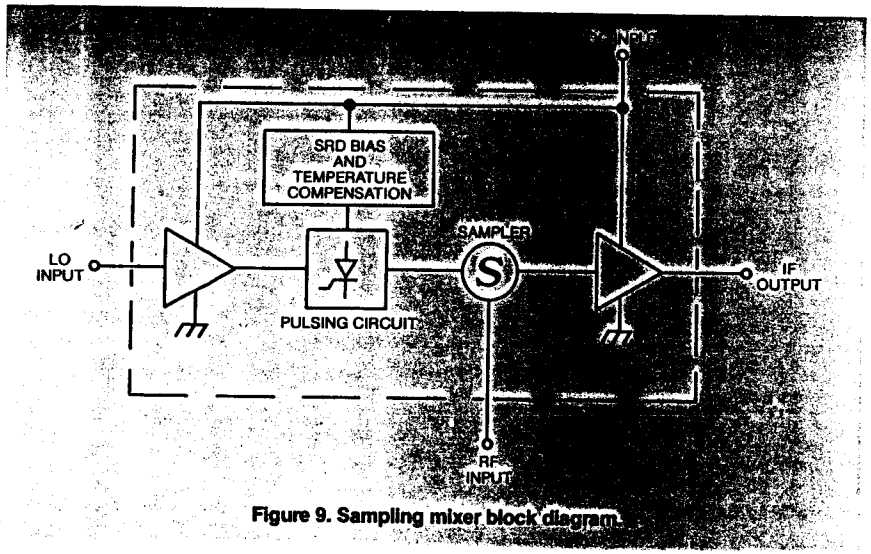
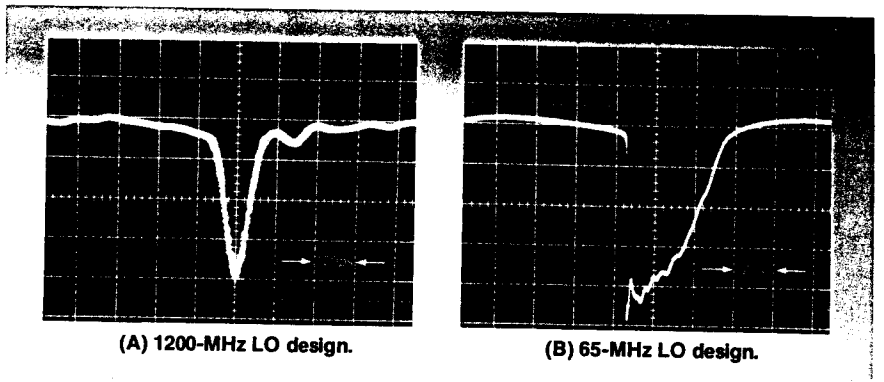


Figure 9. Sampling mixer block diagram.



(A) 1200-MHz LO design. **(B) 65-MHz LO design.**

Figure 10. SRD-generated pulse.

consists of a simple thermistor/resistor arrangement. The element values are chosen after taking dc bias measurements, while optimizing the conversion loss at +85°C, +25°C and -55°C.

The sampler itself is built up on a 15-mil fused-silica substrate. The diodes are beam-lead Schottky-barrier mixing diodes chosen for their low turn-on barrier and low capacitance. The sampling capacitor, being in series with the diode RF "on" resistance, was selected according to a maximum RC time constant for 18-GHz operation.

The input LO-buffer amplifier and the output IF-gain amplifier are cascadable amplifiers chosen for the correct frequency range, power output, gain, etc., as required. Their placement in close proximity to the other circuitry helps to maintain performance and to provide the customer with well-behaved input/output ports. The only output filtering is the natural gain roll-off of the IF amplifiers. The IF bandwidth specification is actually the functional information bandwidth, since the sampling process will generate redundant replicas of the RF input, beyond one-half the LO frequency, as shown in Figure 4.

Sampler Performance

Typical sampler performance is summarized in Table 1 for the low-

	WJ-6221-2	WJ-6222-1
RF	1.8-18 GHz @ -10 dBm	0.2-18 GHz @ -10 dBm
LO	1.2-1.5 GHz @ +10 dBm	60-70 MHz @ -3 dBm
IF	10-500 MHz	3-30 MHz
Conversion Loss	20 dB Typical	20 dB Typical
Spurious	-25 dBc Typical	-22 dBc Typical
IF VSWR	2:1	2:1
RF VSWR	2.5:1	2.5:1
LO VSWR	2:1	2:1

Table 1. Typical sampler performance.

frequency LO version (WJ-6222-1) and for the high-frequency LO version (WJ-6221-2). Both units have an overall dimension of 2.25 x 0.85 x 0.5 inches, and require +15V at 150 mA dc power. They are hermetically sealed and are temperature compensated for operation over -55°C to +85°C, with a conversion loss window (over temperature) of about 3 dB.

Figure 11A shows a typical conversion-loss versus RF-frequency plot. The slight increase in conversion loss as the RF frequency increases is thought to be caused by a combination of a non-ideal sampling pulse, degradation at the RF transition, and increased RF loss through the sampler diodes. Figures 11B and 11C show spurious response and IF baseband flatness, respectively. The flatness measurement was obtained by sweeping the RF over a narrow portion of its frequency range with the spectrum analyzer's persistence turned up. The IF spectrum is a complicated function of how well the sampler can sample-and-hold, as opposed to sampling and discharging.

The IF combining circuit determines the discharge rate of the sampling capacitors and, therefore, will affect both conversion loss and spurious response to some extent. The spurious content of the IF output is an intrinsic characteristic of the sampling process itself. The spurious tones that have proven to be detrimental to a typical system's performance have been recognized, and a specification put on their maximum level. The responses depicted in Figure 11 are typical of both units, the WJ-6221-2 and the WJ-6222-1.

Conclusion

A 2 to 18 GHz downconverter has been constructed utilizing sample-and-hold techniques. Its low cost, low-power requirement, and small package size make it an ideal alternative to YIG-multiplier or harmonic-generator methods of downconversion when used in phase-locked synthesizers or microwave instrumentation applications.

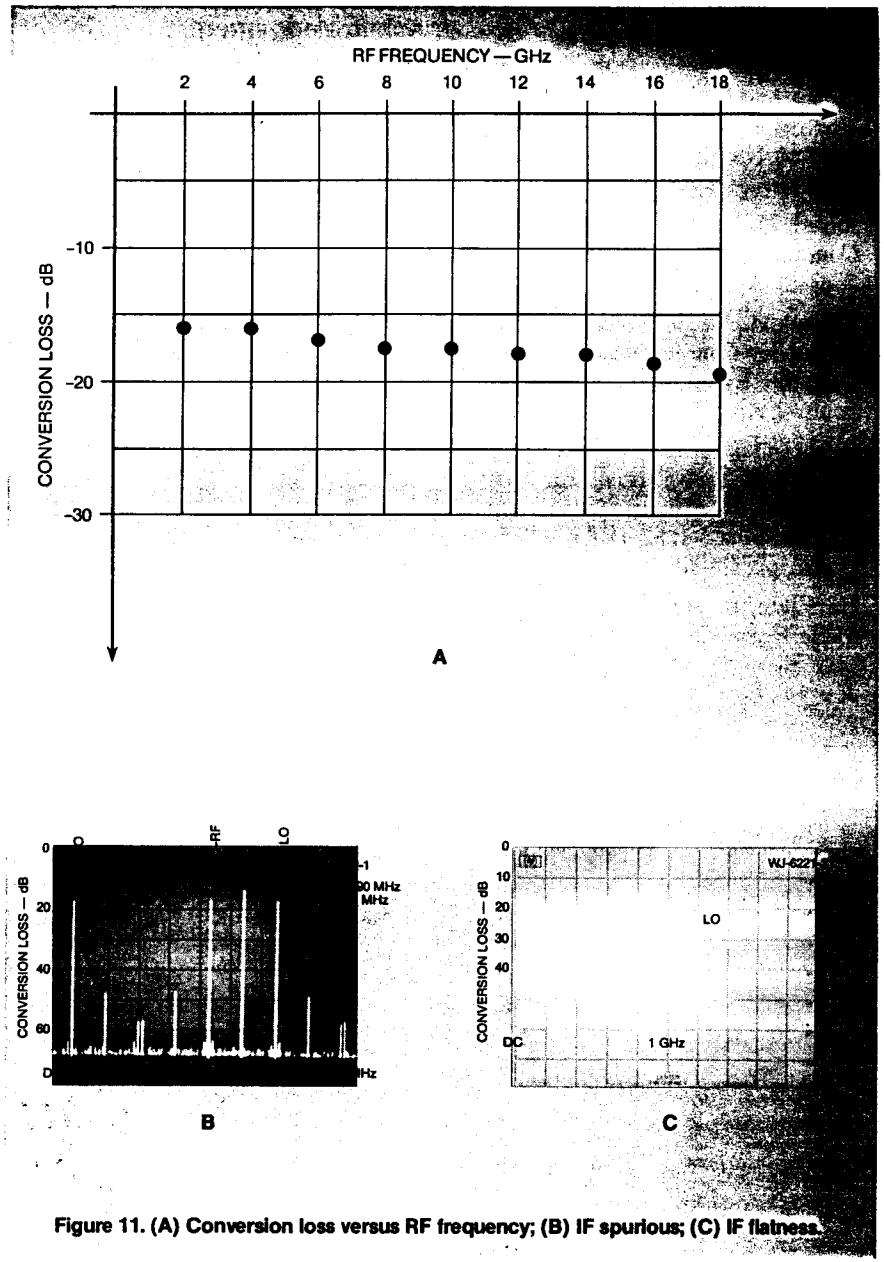


Figure 11. (A) Conversion loss versus RF frequency; (B) IF spurious; (C) IF flatness.

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Before coming to W-J he spent two years with GTE Lenkurt's microwave development department working with microwave radios for telecommunication applications. Steve is presently attending the University of Santa Clara, part-time, working toward an M.S. degree in Engineering Management. He received a B.S.E.E. degree from the University of California, Berkeley.